9^{th} LETI Memory Workshop

June 27, 2017

Embedded Non-Volatile Memory Evolution and Revolution

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STMicroelectronics

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Outline

- Introduction
- Embedded NVM Evolution
- It’s Time for Disruptive Innovation
- Embedded Phase Change Memory
- Summary

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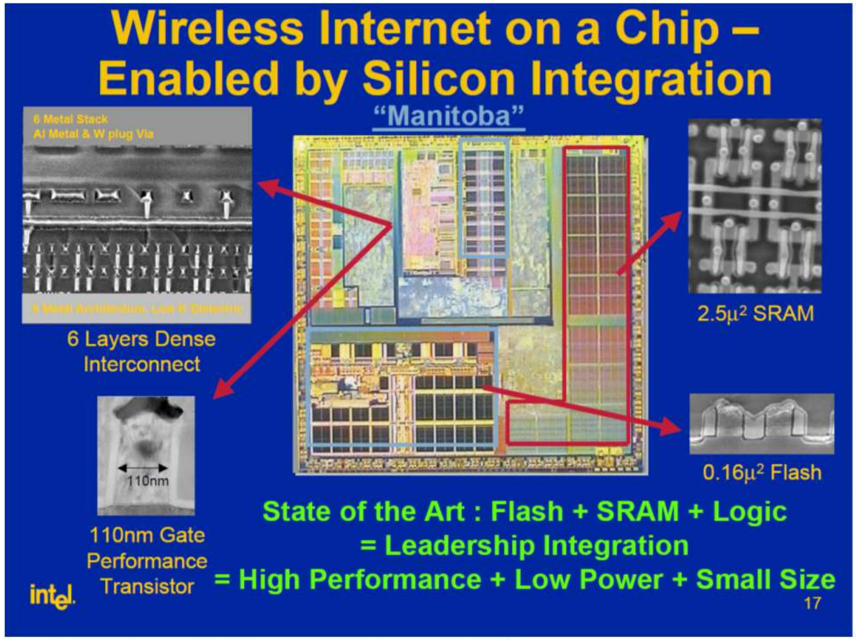
2003: Intel Manitoba Project



Wireless Internet on a Chip – Enabled by Silicon Integration

"Manitoba"

6 Layers Dense Interconnect

2.5µ² SRAM

0.16µ² Flash

110nm Gate Performance Transistor

State of the Art : Flash + SRAM + Logic
= Leadership Integration
= High Performance + Low Power + Small Size

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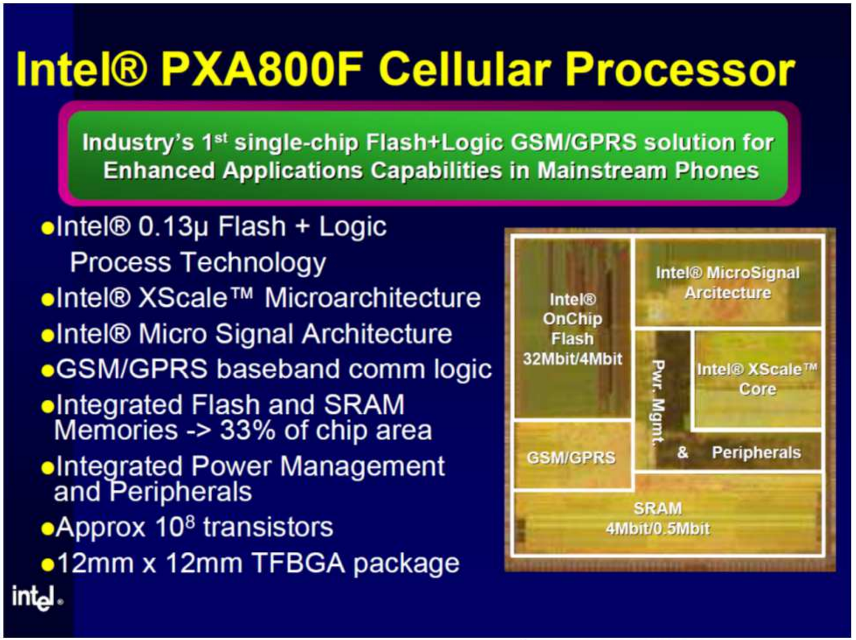
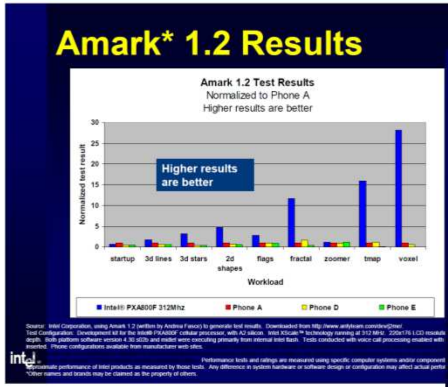


Intel® PXA800F Cellular Processor

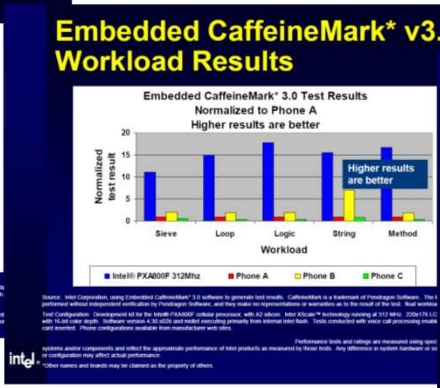
Industry's 1st single-chip Flash+Logic GSM/GPRS solution for Enhanced Applications Capabilities in Mainstream Phones

- Intel® 0.13µ Flash + Logic Process Technology
- Intel® XScale™ Microarchitecture
- Intel® Micro Signal Architecture
- GSM/GPRS baseband comm logic
- Integrated Flash and SRAM Memories -> 33% of chip area
- Integrated Power Management and Peripherals
- Approx 10^8 transistors
- 12mm x 12mm TFBGA package



Amark* 1.2 Results

*Other names and brands may be claimed as the property of others.



Embedded CaffeineMark* v3.0 Workload Results

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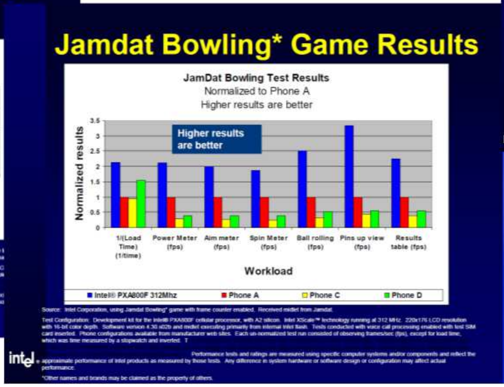

Jamdat Bowling* Game Results

Source: Intel Corporation, using Jamdat Bowling* game with frame counter enabled. Received midlet from Jamdat.

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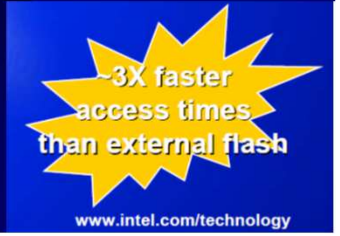
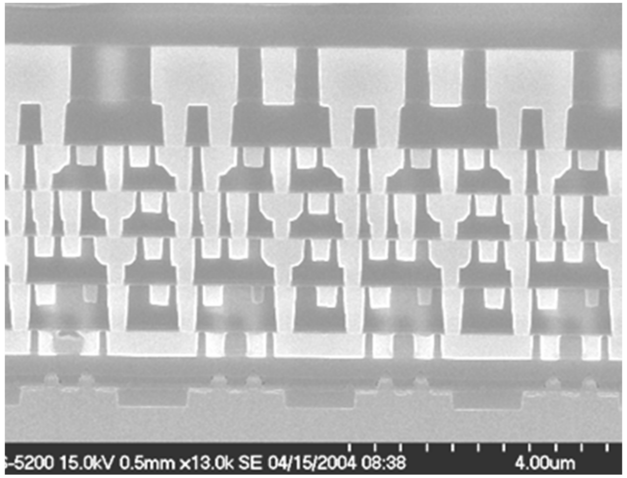
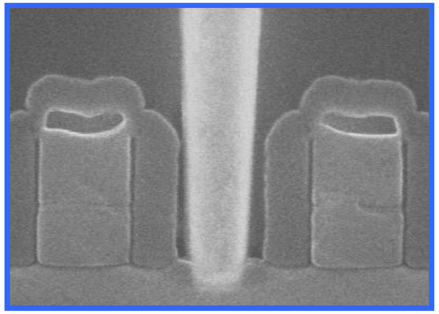
Intel® PXA800F Cellular Processor
Handset Reference Design Phone



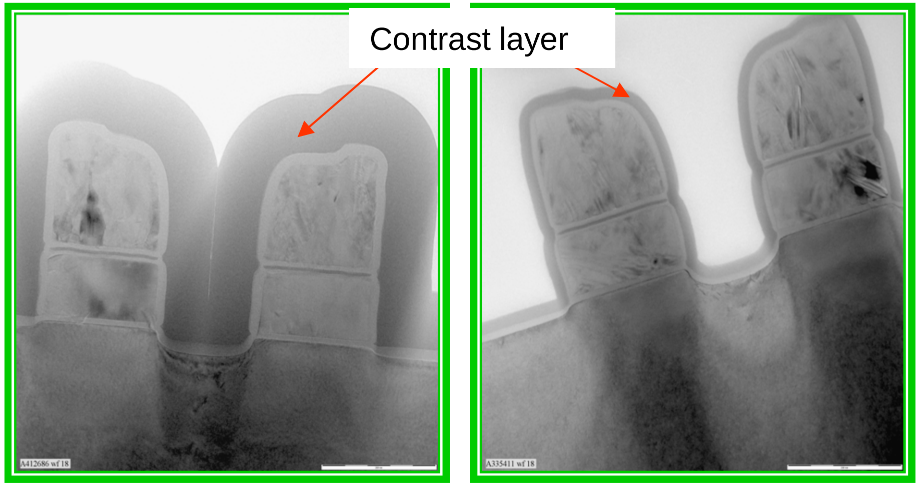
www.intel.com/technology

2003: 130nm ST Embedded NVM





0.16 µm^2 Memory Cell



stand-alone process flow **embedded process flow**

2003: the “Ideal” Convergence Time

- Embedded NVM demand driven by the largest consumer application
- Most advanced stand-alone NVM technology (130nm NOR) featuring low voltage transistors similar to the ones of state-of-the-art logic CMOS technology
- Two major NOR Flash memory players (Intel and ST) providing embedded NVM technology for system-on-chip integration “with no compromises” (best NVM with best CMOS at best cost and best performance)
- Two slightly different integration approaches:
  - Intel: same process flow of stand-alone memory with 3 additional metal layers and improved LV transistors; dedicated effort to develop a specific cell library on “modified” NOR Flash process
  - ST: specific integration flow to embed the same NOR Flash cell of stand-alone memory in the 130nm logic process, ensuring 100% IP reuse

What Happened Next?

- Mobile phones became “smart”
  - PC-like architecture (CPU + DRAM + SSD)
  - no longer demand for super-integration
  - embedded NVM were left without a killer consumer application to drive volumes
- Stand-alone NOR Flash and advanced logic processes started to diverge significantly
  - Lack of process flow synergies
  - Increasing complexity for embedding NVM in advanced logic processes
- Design and manufacturing disaggregation
  - Major stand-alone NVM players disengaged from e-NVM business
  - Proliferation of dedicated NVM solutions for embedded applications
  - Progressive migration from IDM dominated business to IP-provider/fabless/foundry ecosystem

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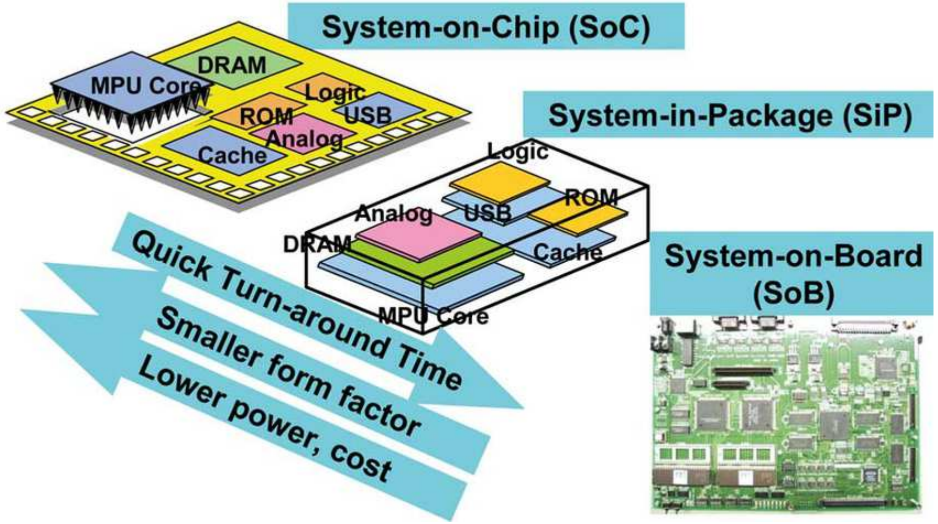
System-On-Chip vs. System-In-Package: a Never-ending Tedious Debate



	System-on-chip	System-in-package
Power	Low	Medium-high
Performance (clock speed)	High	Medium
Design flexibility (features)	High	Low-medium
System design flexibility	Low	High
IP availability	Medium	High
Unit cost	Low	Medium-high
Development cost/Time	High	Low-medium
EDA tools	Mature	Limited
Available design services	High	Limited

- On-chip super-integration and multi-chip-packaging are complementary technologies:
  - They both bring significant advantages in their own best area of application
  - They both have enough business demand to justify their development effort
  - None of the two will ever cannibalize the other one

Main Applications for e-NVM

- Automotive SoC's
  - Super-integration driven by performance and reliability
  - Leading eNVM technology road-map for memory capacity and advanced CMOS
  - Most demanding as far as reliability and operating temperature range

- Smart Cards (Secure Micro)
  - They are intrinsically NV memory based single-chip systems
  - Most sensitive to eNVM cell size and process cost
  - Require very low energy programming for contact-less applications

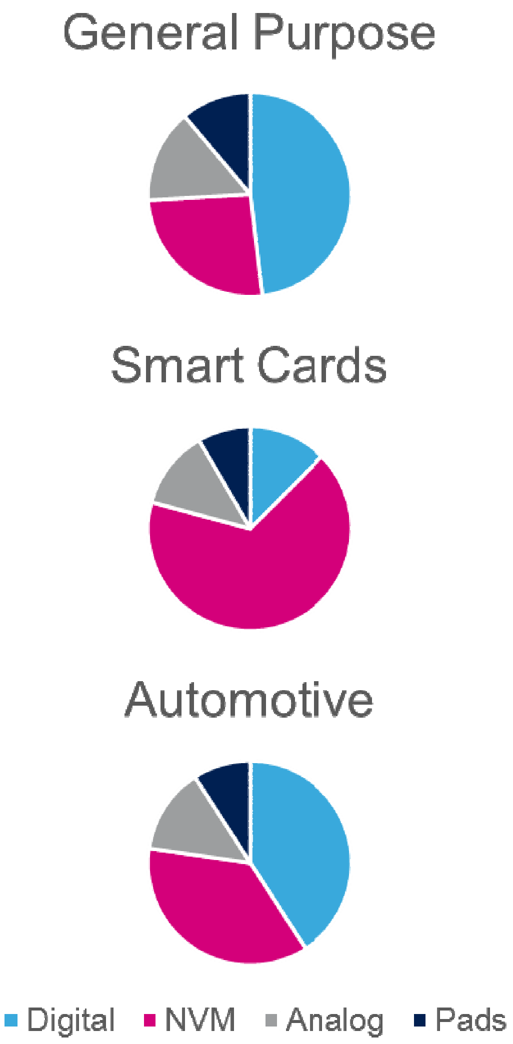
- General Purpose Microcontrollers (MCU)
  - Embedded NVM needed for flexibility (for both code and data)
  - Broad range of applications and large end-customer base

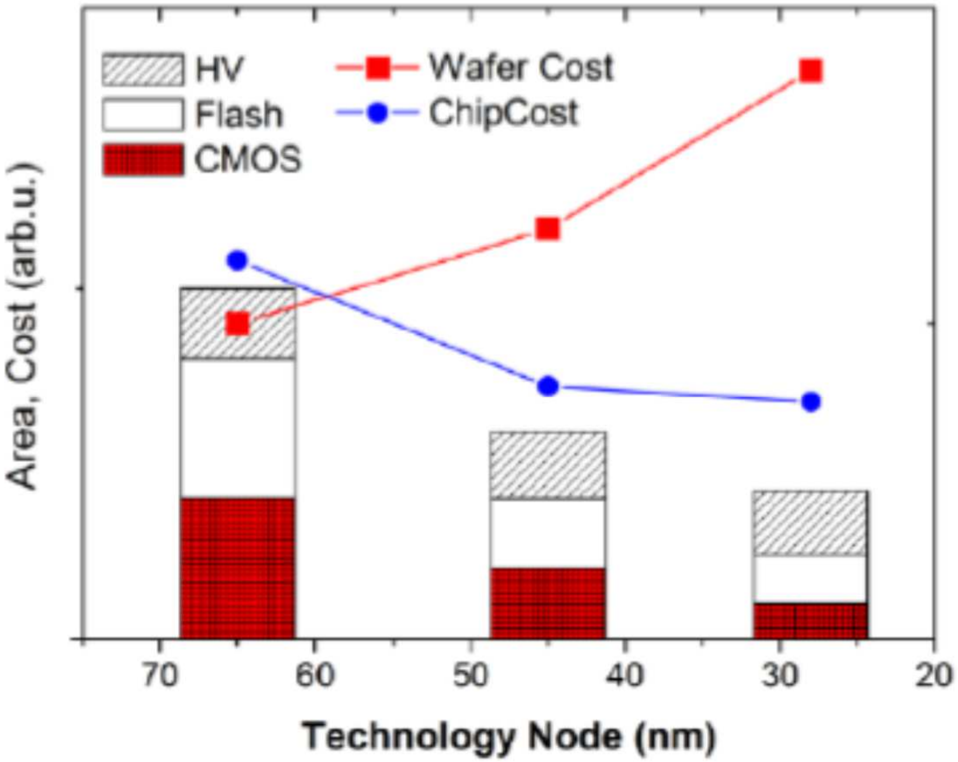
IoT: the next attractive opportunity!

Key Specs for Main e-NVM Applications

Application	MCU	SIM Smart cards	IoT	Auto
Operation Temperature	-40C ~ 125C	-40C ~ 85C	-40C ~ 125C	-40C ~ 165C
Bus Width	x32 / x64	x32 / x38	x32	x144
Standby Current	<1µA @ 25C	<1µA @ 25C	<1µA @ 25C	<1µA @ 25C
Read Current	<5mA / 33MHz	<5mA / 33MHz	<2 mA / 40MHz	<40mA / 200MHz
Access Time	<20ns	<40ns	<25ns	<15ns
Endurance	10K	500K	100K	500K
Data Retention	10yrs	10yrs	10yrs	10yrs
Soldering (a few min. @ 260C)	Yes	Yes	Yes	Yes

Chip Area Partitions and Cost Trends





R. Strenz, IEDM 2011

Main e-NVM Technologies

- EEPROM
  - + Writing power (F-N tunneling)
  - + Reliability
  - + Bit granularity
  - - Cell size (2T cell)
  - - 15V writing

Low-End products

mainly driven by cost

- 1T NOR Flash
  - - Writing power (CHE programming)
  - + Reliability
  - - Sector/page granularity
  - + Cell size (1T cell)
  - - 10V writing

High-End products

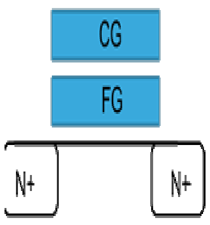
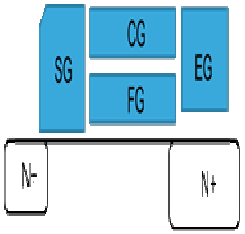
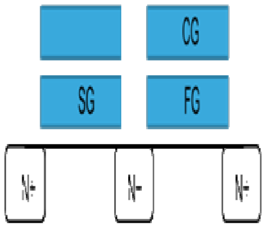
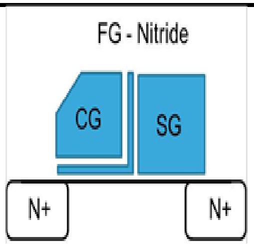
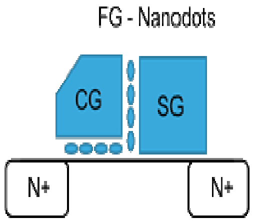
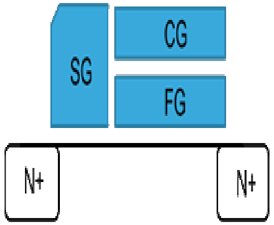
mainly driven by high array density and fast random access

- Split-gate Flash
  - + Writing power (Source Side Injection)
  - - Endurance (design help needed)
  - + Access time
  - + Page granularity
  - - Cell size (1.5T cell)
  - - > 10V writing
  - - Process complexity

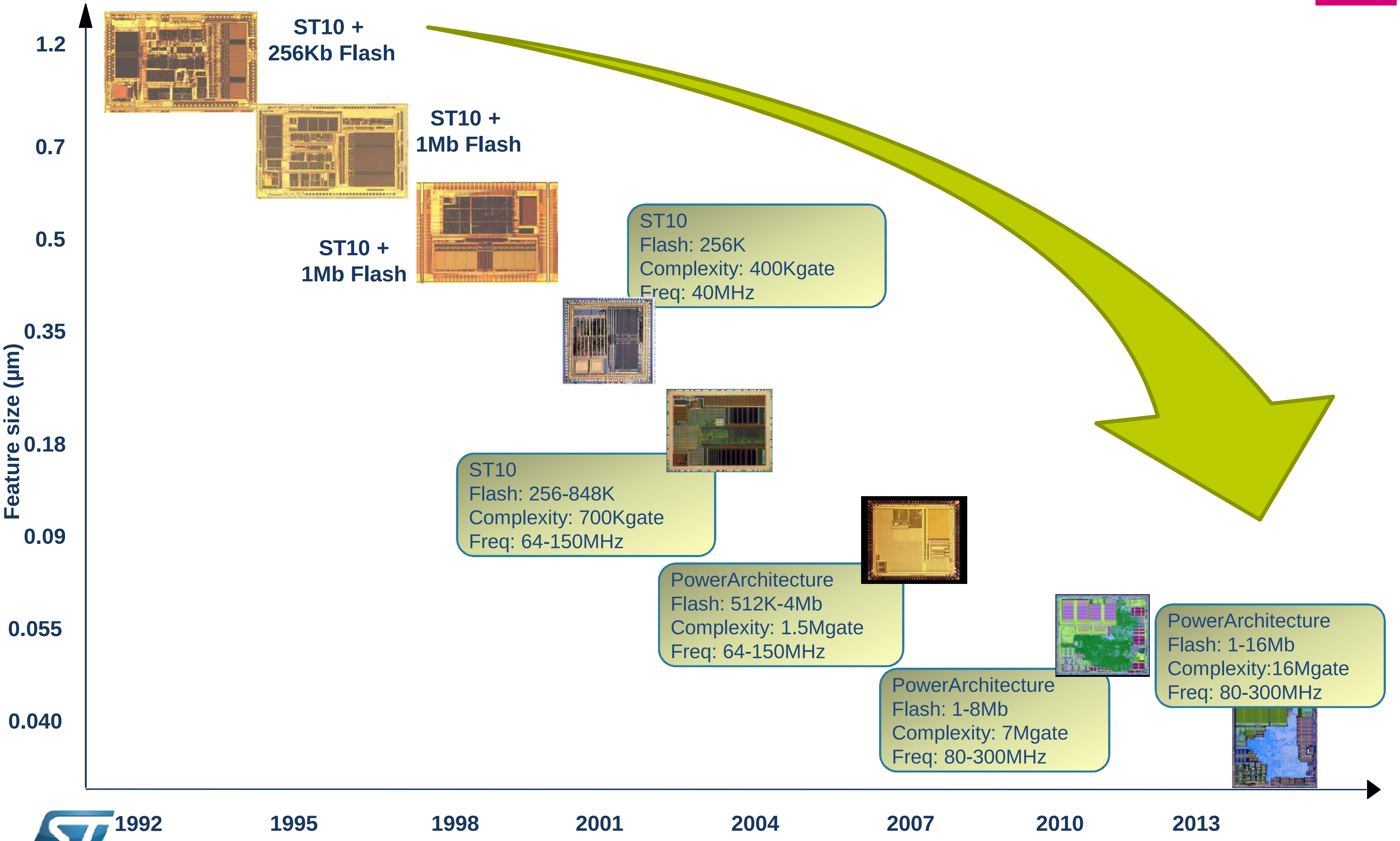
Low Power products

mainly driven by power consumption

Most Adopted e-Flash Memory Cells

Type	1T NOR	1.5T (ESF3)	2T	1.5T MONOS	1.5T TFS	1.5T HS3P
Device structure						
P/E mechanism	CHE / FN	SSI / FN	FN / FN	SSI / HHI	SSI / FN	SSI / FN
PRO's	High density	Power, LV reading path	Power	Power, LV reading path	Power, LV reading path	Power
CON's	Power	Process complexity	Scalability	Reliability	Relatively mature concept	Process complexity

ST Automotive Microcontrollers with e-Flash



ST10 +
256Kb Flash

ST10 +
1Mb Flash

ST10 +
1Mb Flash

ST10
Flash: 256K
Complexity: 400Kgate
Freq: 40MHz

ST10
Flash: 256-848K
Complexity: 700Kgate
Freq: 64-150MHz

PowerArchitecture
Flash: 512K-4Mb
Complexity: 1.5Mgate
Freq: 64-150MHz

PowerArchitecture
Flash: 1-8Mb
Complexity: 7Mgate
Freq: 80-300MHz

PowerArchitecture
Flash: 1-16Mb
Complexity:16Mgate
Freq: 80-300MHz

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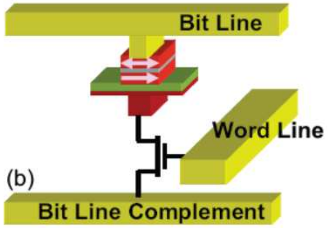
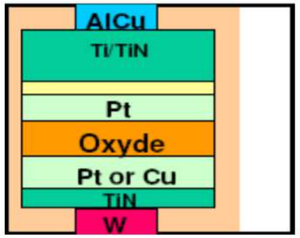
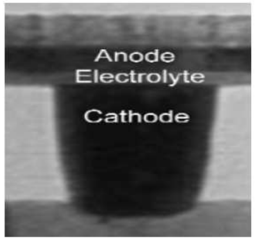
CMOS Roadmap Discontinuity

- CMOS technology has undergone several disruptive innovations to support MOS transistor scaling
  - High K gate dielectrics
  - Metal gate
  - Fully Depleted SOI
  - Fin FET
  - …

- Embedding Floating Gate NVM’s has become more and more troublesome and costly
  - Process integration complexity
  - 15-20 additional masks
  - Reliability degradation
  - …

- BEOL EM’s have great opportunities at and below 28nm

BEOL e-NVM Cells

Type	STT MRAM	OxRAM	CBRAM	PCM
Device structure				
Maturity	Prototyping	Physical working mechanism and material explorations	Physical working mechanism and material explorations	Production
PRO’s	Fast P/E and access time	Fast P/E time	Fast P/E time	Fast P/E time
CON’s	Stack complexity Sensing window	Maturity	Maturity	Temperature stability

Emerging Memory Key Players

Category	MRAM/STTMRAM	PCM	RRAM
Pioneers	EVERSPIN TECHNOLOGIES CROCUS Technology Blossoming future avalanche technology Spin Programmable Storage Solutions		adesto TECHNOLOGIES Panasonic
Memory IDM	SAMSUNG SK hynix TOSHIBA Micron	Micron SAMSUNG SK hynix intel WD Western Digital MXIC	TOSHIBA SAMSUNG winbond SanDisk SK hynix
Embedded IDM	infineon RENESAS QUALCOMM NXP	ST life.augmented MXIC	infineon RENESAS NXP
Fabless	TDK Spin Transfer Technologies An Allied Minds Company		Crossbar SONY symetrix Weebit Jump into the future
Foundries	tsmc TOWERJAZZ SAMSUNG GLOBALFOUNDRIES		tsmc SMIC TPSCo Because Life is Analog

Embedded Emerging Memory Advantages vs. Conventional (FG or CT) e-Flash

- Low temperature Back-End-Of-Line integration
  - No impact on transistor process flow → easier and faster integration
  - No impact on transistor performance → 100% IP reuse

- Lower programming voltage
  - Possibility of using medium voltage transistors already available in std CMOS

- Lower number of additional masks
  - 3-10 additional masks, depending on cell structure and programming voltage

- Better performances
  - 10ns-1µs programming time range
  - 1-100 pJ programming energy range
  - Single bit program granularity (direct over-writing)
  - > 1M writing cycles
  - Virtually immune to radiation effects

Why Emerging Memories Have Not Yet Taken the Lead in the e-NVM Race?

- Major companies, both IDM’s and foundries, have been working on e-EM’s for over 10 years
- EM advantages over conventional flash memories were evident and valid also for conventional CMOS, before the most recent disruptive innovations
- Two major concerns have limited so far the adoption of e-EM’s:
  - Lack of confidence on EM maturity, manufacturability and reliability due to poor stand-alone memory track record
  - Limited high temperature operation range

… but CMOS disruption is now calling for change!

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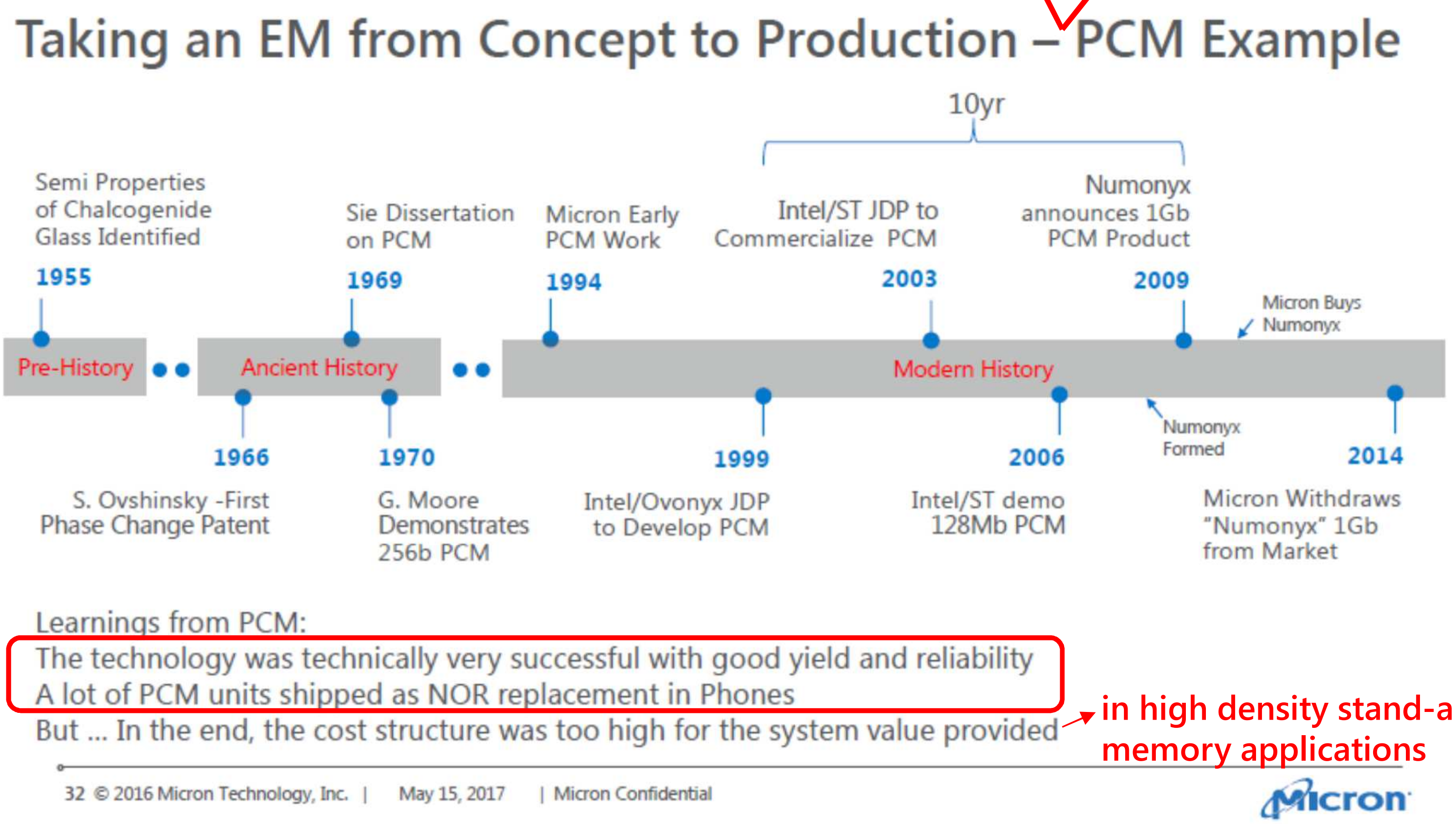
PCM Stand-Alone Memory History



Taking an EM from Concept to Production – 1T/1R PCM Example

10yr

1955 Semi Properties of Chalcogenide Glass Identified

1966 S. Ovshinsky -First Phase Change Patent

1969 Sie Dissertation on PCM

1970 G. Moore Demonstrates 256b PCM

1994 Micron Early PCM Work

1999 Intel/Ovonyx JDP to Develop PCM

2003 Intel/ST JDP to Commercialize PCM

2006 Intel/ST demo 128Mb PCM

Numonyx Formed

2009 Numonyx announces 1Gb PCM Product

Micron Buys Numonyx

2014 Micron Withdraws "Numonyx" 1Gb from Market

Learnings from PCM:

The technology was technically very successful with good yield and reliability

A lot of PCM units shipped as NOR replacement in Phones

But ... In the end, the cost structure was too high for the system value provided → in high density stand-alone memory applications

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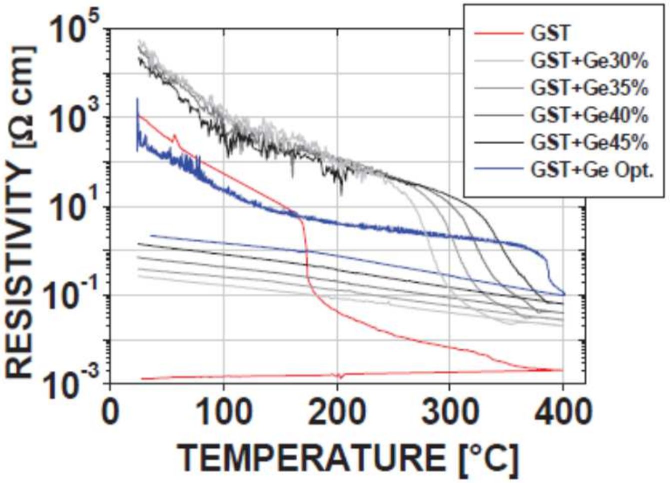
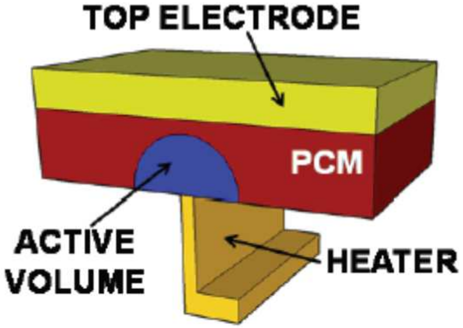
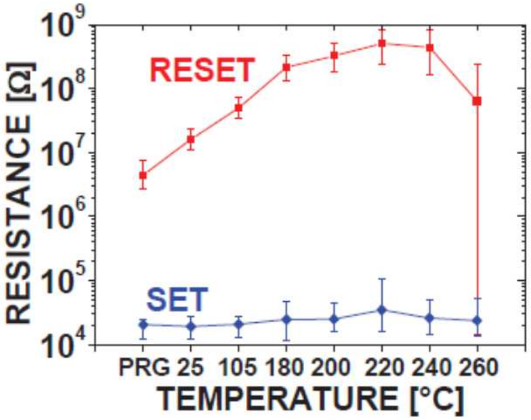
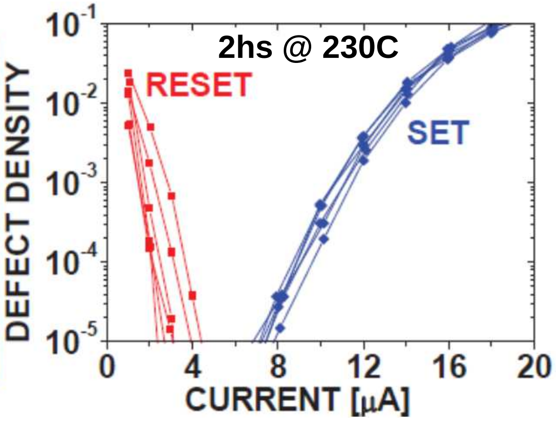
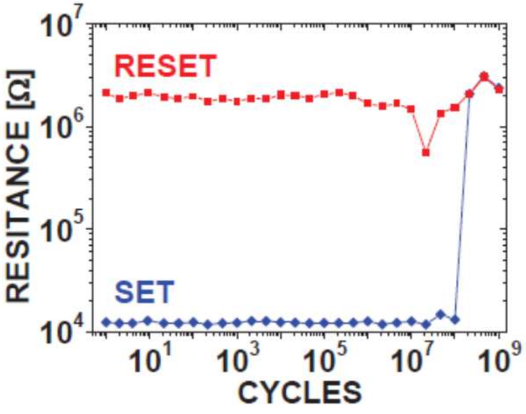
ePCM for Automotive Applications





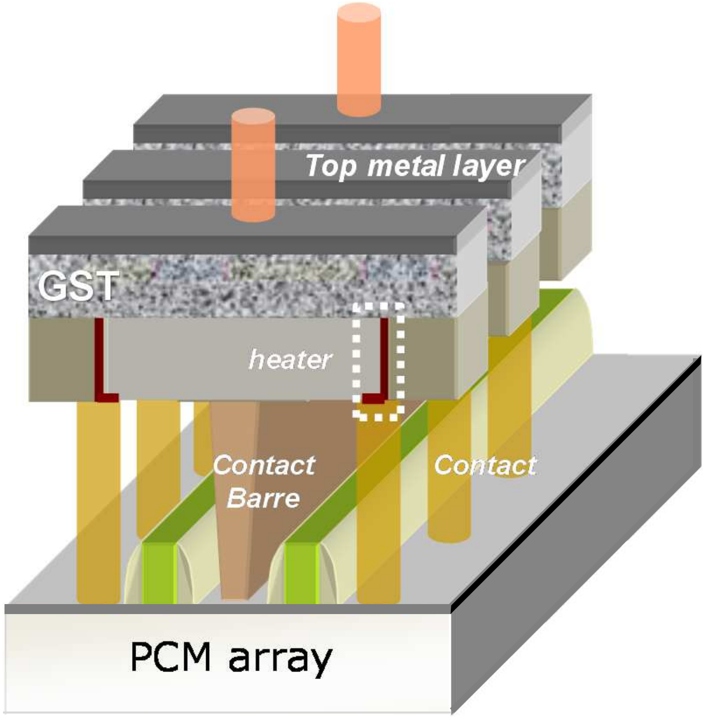


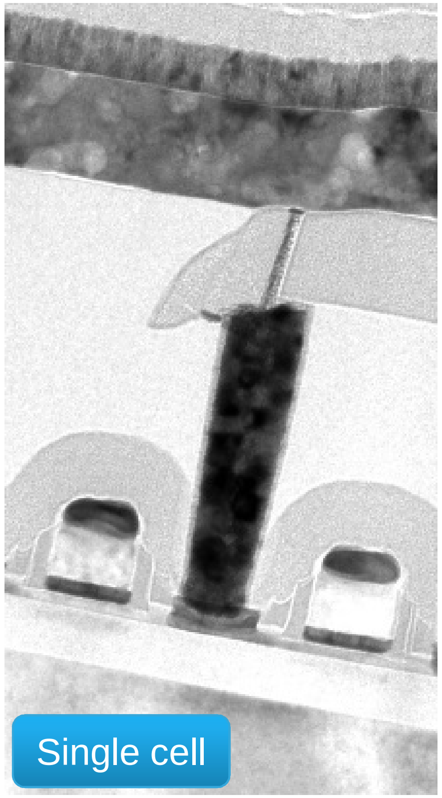




V.Sousa et al, Symposium on VLSI Technology 2015

28nm High-K Metal Gate FDSOI ePCM





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- Emerging Memories show clear advantages over conventional NVM for embedded applications
  - Less additional masks
  - Lower impact on CMOS process front-end (development effort and time to market)
  - Better performance (writing speed, endurance, single bit overwrite
  - Rad-hardness
  - …
- Poor technology maturity and lack of high volume stand-alone manufacturing history has delayed the wide adoption of EMs for embedded applications
- CMOS transition to FDSOI HKMG and to FinFet is making more and more costly and difficult to embed conventional NVMs
- EMs have great opportunities to become mainstream at and below 28nm
- Data retention at high temperature and soldering capability will be two of the most relevant features for selecting the winner

Thanks for your attention!

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